Design of Analog Integrated Systems (ECE 615)

Lecture 9
SAR and Cyclic (Algorithmic) Analog-to-Digital Converters

Ayman H. Ismail
Integrated Circuits Laboratory
Ain Shams University
Cairo, Egypt
ayman.hassan@eng.asu.edu.eg

Outline

• SAR ADC
  – The binary search
  – Charge re-distribution SAR ADC
  – The sampling Phase
  – The hold Phase
  – Bit-cycling
• Practical Considerations
• Performance Limits
• Multiple-bit SAR
• Monotonic Switching
• Monotonic Switching with constant CM
• State of the art
• Cyclic (Algorithmic) ADC
Successive-Approximation Converters

- SAR ADC converters can achieve relatively high accuracy, at very low power.
- SAR ADC converters require only modest circuit complexity.
- In the simplest cases requiring only a single comparator, a bank of capacitors with switches, and a small amount of digital control logic.
- Theory of operation depends on binary-search using DAC

Binary Search

- 6-bits binary search
Charge Redistribution SAR ADC

- Composed of comparator, capacitive DAC and control logic
- \( C_{1A} = C_{1B} = C, C_2 = 2C, C_3 = 4C, C_{B} = 2^{B-1}C \)
- Operation is composed of two main phases:
  - Sampling phase
  - Hold phase (may be merged with the first step of bit cycling)
  - Bit-cycling phase

The Sampling Phase

- \( V_{in} \) is sampled on all DAC capacitors
- \( V_{x} = 0 \)
- \( Q = -V_{in} \cdot 32C = -V_{in} \cdot C_{total} \)
The Hold Phase

\[ C_{\text{total}}(V_x - 0 - (0 - V_{\text{in}})) = C_p (0 - V_x - 0) \]

\[ V_x = \frac{-C_{\text{total}}}{C_{\text{total}} + C_p} V_{\text{in}} \]

Bit-Cycling Phase: The MSB

- Comparison to Mid-scale

\[ \frac{C_{\text{total}}}{2}[(V_{\text{ref}} - V_x) - (0 - \frac{-C_{\text{total}}}{C_{\text{total}} + C_p} V_{\text{in}})] = (\frac{C_{\text{total}}}{2} + C_p)(V_x - 0) - (\frac{C_{\text{total}}}{C_{\text{total}} + C_p} V_{\text{in}} - 0) \]

\[ \frac{C_{\text{total}}}{2} V_{\text{ref}} - \frac{(C_{\text{total}} + C_p)}{(C_{\text{total}} + C_p)} C_{\text{total}} V_{\text{in}} = (C_{\text{total}} + C_p)V_x \]

\[ V_x = \frac{C_{\text{total}}}{(C_{\text{total}} + C_p)} \frac{V_{\text{ref}}}{2} - V_{\text{in}} \]
Bit-Cycling Phase: The MSB

- Comparison to Mid-scale
- \( V_x < 0 \Rightarrow V_{in} > 0.5V_{ref} \Rightarrow \text{Bit5}=1 \)
- \( V_x > 0 \Rightarrow V_{in} < 0.5V_{ref} \Rightarrow \text{Bit5}=0 \)

Bit-Cycling Phase: The Following Bit (Assuming MSB=0)

- \( V_x < 0 \Rightarrow V_{in} > 0.25V_{ref} \Rightarrow \text{Bit4}=1 \)
- \( V_x > 0 \Rightarrow V_{in} < 0.25V_{ref} \Rightarrow \text{Bit4}=0 \)
**Signal at Comparator Input**

- $V_{in} - \Sigma V_{DAC \text{-steps}} \rightarrow \text{zero (<LSB)}$
- This is the differential version of slide 4

---

**Practical Consideration**

- The parasitic cap, $C_p$, attenuates $V_x$, and hence, the comparator decision becomes more sensitive to comparator offset.
- However, more important $C_p$ is a non-linear capacitor that deteriorates linearity of the ADC.
- Therefore, the unit cap $C$ should be selected $>> C_p$.
- Recall that the value of $C$ is determined by matching requirements (N-bit SAR ADC requires an N-bit DAC).
- In practical realizations, matching requirements may lead to unit cap in the same order of parasitics. To avoid deterioration of performance due to $C_p$, unit cap $C$ is selected higher than the value dictated by matching. In this case, using segmentation can lead to lower DAC area.
Performance Limitations

- Sampling speed is limited by the settling time during sampling and bit-cycling
- Bandwidth is limited by the bandwidth of the sampling circuit network during sampling and bit-tests
- Comparator offset directly leads to an ADC offset
- INL and DNL of ADC depends on DAC INL and DNL
- Power dissipation is mainly due to comparator and reference voltage buffer (charging/discharging capacitive DAC)

Multi-bit SAR ADC

- Conventional SAR compares input to a single reference value each conversion step, and hence, divides the search space into two on each clock cycle
- by performing multiple comparisons on each clock cycle, and dividing the search space up into smaller regions, more than one bit is resolved per cycle, and less number of clock cycles is needed per conversion.
- The resulting structure becomes flash-like.
- Comparator offset mismatch results in INL and DNL as in the case of flash ADC
Multi-bit SAR ADC

Zhiheng Cao, Shouli Yan, Member, IEEE, and Yunchu Li, Member, IEEE, "A 32 mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13um CMOS," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 3, MARCH 2009.

Monotonic Switching Scheme SAR ADC

- Conventional switching
  - Non-monotonic. DAC capacitors are switched to Vrefp and may be re-switched to Vrefn based on comparator decision
  - Inefficient capacitor network switching energy
- Monotonic switching [Liu (Cheng-Kung Uni.), JSSC10]
  - MSB capacitor of the DAC array is eliminated. Therefore, the capacitor array is reduced by 50% (power/area saving).
  - DAC capacitors are switched to the right Vrefp or Vrefn based on previous DAC/comparator decision. Hence, no re-switching is needed, and considerable reduction in switching power is saved
  - However DAC signal CM varies during bit cycling
  - Varying CM induces varying comparator offset, and hence non-linearity
Monotonic Switching Scheme SAR ADC

Monotonic Switching Scheme SAR ADC with Constant CM

- Vcm based switching [Maloberti, JSSC10]
  - Monotonic switching, resulting in reduction in capacitor array by 50% and switching power saving
  - Constant DAC signal CM. Hence, non-linearity avoided
  - The DAC capacitors are initially connected to the reference voltage CM and is switched to Vrefp or Vrefn based on comparator previous decision

---

Monotonic Switching Scheme SAR ADC with Constant CM

Typically, the SAR architecture was used for high-accuracy (12-16 bit) low speed (<1MHz) ADCs.

However, in the last decade SAR ADC was used to implement medium to low accuracy ADCs (≤10-bit) working at ~ 100MHz, and ~ GHz when time interleaving is employed.
Cyclic (Algorithmic) ADC

- Cyclic ADC can be regarded as

- An ADC that operates with the same principle of pipelined ADC. However, a single stage is used in a cyclic fashion instead of using several stages. Therefore cyclic ADC needs many clock cycles per conversion

OR

- An ADC that operates in a similar way to successive-approximation converter. However, whereas a successive-approximation converter halves the reference voltage in each cycle, an algorithmic converter doubles the error voltage while leaving the reference voltage unchanged.

Cyclic ADC Block Diagram

- \(-V_{\text{ref}}/2 < V_{\text{in}} < V_{\text{ref}}/2\)
- One bit resolved every cycle
- Advantages: Area efficient and simple to calibrate
- Disadvantages: Low throughput (n+1 clock cycles for n bits) compared to pipelined ADC. Also it is sub-optimal regarding power efficiency because no scaling of stages can be used as in ADC.
### References

- B. Murmann, EE315A(VLSI Signal conditioning circuits) Handouts, Stanford University
- A. H. Ismail “SAR ADC Survey” 2011
- Zhiheng Cao, Shouli Yan, Member, IEEE, and Yunchu Li, Member, IEEE,” A 32 mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13um CMOS,” IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 3, MARCH 2009.